REMARKS

Claims 1-14 are currently pending. The Examiner's rejections are traversed below.

On page 2 of the Office Action, the Examiner rejected claims 1-5, 7, 9 and 14 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,771,243 (Lee).

Lee is directed to a technique for identifying redundant test patterns, which allegedly leads to the reduction of the number of test patterns for integrated circuit devices. According to Lee, the test results of a sample of products are analyzed. Lee states that the basic idea for identifying potentially redundant test patterns is to locate a set of test patterns which can be replaced by another set of test patterns containing one or more test patterns. *See* Lee, column 2, lines 25-34.

In at least one embodiment of the present invention, a selection device selects essential test stimuli from among subsets of the set of test stimuli after mapping between the test stimuli and the faults has been established by the simulation. An elimination device eliminates redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset. *See* claim 1, for example.

Applicants respectfully submit that independent claims 1 and 14 are patentable over Lee, as Lee fails to disclose, "an elimination device *eliminating redundant test stimuli* from among subsets of test stimuli *after selection of essential test stimuli* from each subset," as recited in claim 1, for example.

In contrast to the present invention, Lee simply describes a method for identifying redundant test patterns. Lee is silent regarding selecting essential test stimuli from a subset. For example, Lee states that the results of two sets of test patterns such as set A and set B are selected from the testing of a product where each test set can contain one or more different patterns. Lee does not indicate whether essential test stimuli from subsets of the test patterns are selected.

Applicants respectfully submit that there is another fundamental difference between Lee and the present invention. The present invention is concerned with generating patterns of a smallest possible number with which it is still possible to conduct a series of tests that cover all the conceivable types of faults. In contrast, Lee is concerned with removing a test pattern that is determined ineffective by analyzing a result of an actually conducted measurement. According to the method adopted in Lee, a test pattern comes to be removed even if it is capable of detecting a type of fault, unless the occurrence frequency of the associated type of fault is high

enough with chips that are actually put to the tests. For this reason, in Lee, the saving in the testing costs is more important than the quality of the conducted tests, and consequently, it is directed to testing chips of other types than the types used for the present invention.

Further still, the present invention takes a logical approach and employs simulation of a fault for finding out a presence of a fault while Lee takes an analytical approach and collects data of faults experienced in actual measurements on chips.

Therefore, independent claims 1 and 14 are patentable over Lee, as Lee does not disclose, "an elimination device eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset," as recited in claims 1 and 14, for example.

As dependent claims 2-5, 7, and 9 depend from independent claim 1, the dependent claims are patentable over Lee for at least the reasons presented for the independent claims.

On page 4 of the Office Action, claim 14 was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,810,372 B1 (Unnikrishnan).

Unnikrishnan is directed to generate a minimum set of test patterns that allegedly still fulfills the predetermined operational conditions (events). The invention is apparently concerned with taking in a number of random patterns as an initial set of test patterns and then executing processes designed so as to follow a genetic algorithm for bringing in additional patterns, evaluating patterns and removing away certain patterns for eventually arriving at such a set of test patterns. The section of the reference identified by the Examiner is concerned with removing a test pattern which is discovered to be one that covers an event that has already been covered when tested by using another pattern.

The Examiner alleged that Unnikrishnan teaches substantially the invention as claimed in claim 14.

Applicants respectfully submit that the selection identified in operation 204 relates to the selection of all tests from a population and is not tantamount to a selection of "essential test stimuli from each subset," as in the present invention. Moreover, Unnikrishnan clearly indicates that the selection of all tests occurs from the population, that is, the original set, not a subset of a set.

Therefore, claim 14 is patentable over Unnikrishnan.

On page 4 of the Office Action, claims 1-5 and 7-14 were rejected under 35 U.S.C. § 102(b) as being anticipated by "Cost-Effective Generation of Minimal Test Sets for Stuck-at Faults in Combinational Logic Circuits," IEEE, Dec. 1995, pp. 1496-1504 (Kajihara).

On page 8 of the Office Action, the Examiner stated that, "one can understand that the removal cannot be done before selection. Nothing to remove if there is no selection." Applicants respectfully submit that the Examiner's assertions are simply untrue. In Kajihara, the double detection procedure occurs first. In other words, in Kajihara, redundant tests are dropped first. After the redundant tests are dropped in Kajihara, the essential faults procedure then occurs.

The Examiner is incorrect to state that removal cannot be done before selection and is also incorrect in stating that there is nothing to remove if there is no selection. For example, Applicants submit that there is something to remove even though selection has not occurred. In particular, redundant tests are removed or dropped in Kajihara, even though no selection of *essential* faults has occurred prior to removal of the redundant tests. Therefore, in contrast to the present invention, Kajihara clearly drops redundant tests first, then executes an essential faults procedure.

In light of the foregoing, independent claims 1 and 10-14 are patentable over Kajihara, as Kajihara fails to disclose the above-identified feature of the claims of the present invention.

On page 7 of the Office Action, claim 6 was rejected under 35 U.S.C. § 103(a) as being obvious over Kajihara.

Applicants respectfully submit that Kajihara teaches away from the present invention in that Kajihara clearly drops redundant tests firsts, then executes an essential faults procedure. Therefore, in Kajihara, there is no suggestion of, "eliminating redundant test stimuli from among subsets of test stimuli after selection of essential test stimuli from each subset," as recited in claim 6, via, claim 1.

The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

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